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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,595	08/30/2001	Gary L. Swoboda	TI-30482	2423

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EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,595	SWOBODA, GARY L.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 have been presented for examination based on the application 09/943595 filed on 30 August 2001.

Priority

2. This application appears to be a division of Application No. 09798561, filed 2nd March 2001. A later application for a distinct or independent invention, carved out of a pending application and disclosing and claiming only subject matter disclosed in an earlier or parent application is known as a divisional application or "division." The divisional application should set forth the portion of the earlier disclosure that is germane to the invention as claimed in the divisional application. Application No. 09798561 further claims priority from provisional Applications No. 60186326 & 60219340, filed on the 2nd March 2000.

Information Disclosure Statement

3. An initialed and dated copy of Applicant's IDS form 1449 is attached to the instant Office action.

Oath/Declaration

§ 1.48 Correction of inventorship in a patent application, other than a reissue application, pursuant to 35 U.S.C. 116.

> (f)(1) Nonprovisional application —filing executed oath /declaration corrects inventorship. If the correct inventor or inventors are not named on filing a nonprovisional application under § 1.53(b) without an executed oath or declaration under § 1.63 by any of the inventors, the first submission of an executed oath or declaration under § 1.63 by any of the inventors during the pendency of the application will act to correct the earlier identification of inventorship.

4. Examiner acknowledges the request to remove one of the inventors from the inventive entity present in the original application. A new oath/declaration must executed to complete the inventorship change in accordance of 37 CFR 1.48(f)(1) with only the signatures of the one inventor (i.e. Gary L. Swoboda).

Specification

5. This instant application does not contain a summary of invention. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 discloses:

> "A method of exporting emulation information from a data processor, comprising:
> *(a)* collecting internal emulation information within a data processor;
> *(b)* arranging the collected emulation information into a plurality of first information blocks;
> *(c)* receiving the plurality of first information blocks and arranging the emulation information contained therein into a plurality of second information blocks which differ in size from the first information blocks;
> *(d)* and outputting a sequence of the second information blocks from the data processor via a plurality of terminals of the data processor."

Steps (a), (b) & (d) seems to be performed on the data processor. It is not clear form the claim limitation defined in claim 1, what entity is performing the step of receiving and arranging the data (step (c)) into second information blocks. Appropriate correction is required.

Claims 2-15 are rejected for incorporating the deficiencies of claim 1 by dependency.

Examiner respectfully suggests changing the language similar to "transmitting and receiving first information blocks within the data processor and arranging the emulation information contained therein into a plurality of second information blocks which differ in size from the first information blocks;".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-4, 8-9, 15-17 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Edwards, US Patent No 6,732,307.

Regarding Claim 1

Edwards teaches:

> "A method of exporting emulation information from a data processor, comprising:
> collecting internal emulation information within a data processor;"

as a system performing the same steps as method in the claim 1. Edwards teaches that trace emulation information associated with the processor (Edwards: Col. 2, Lines 31-33) is collected in the trace buffers (Edwards: Fig. 2, Elements 102, 105, 227).

Edwards also teaches:

> "arranging the collected emulation information into a plurality of first information blocks;"

as collecting the information in trace buffer and arranging it in a specific format (Edwards: Col. 17, Lines 45-52). The format of the trace information could be fixed or variable.

Edwards also teaches:

> "receiving the plurality of first information blocks and arranging the emulation information contained therein into a plurality of second information blocks which differ in size from the first information blocks;"

as a receiving step that will read information from the trace buffer (Edwards: Col. 17, Lines 40-44) and debug circuit (Edwards: Fig. 2, Elements 103)that will receive the trace information from trace buffer (Edwards: Fig. 2, Elements 227) into trace data latch (Edwards: Fig. 2, Elements 206) via trace data connection (Edwards: Fig. 2, Elements 222). The arranging step is performed in the debug circuit. The data received from the trace buffer (representing the first information block) is formatted to include time stamp information and stored in FIFO (Edwards: Col. 7, Lines 27-31; Fig.2, Element 202). FIFO is storage sequential storage element re-presenting second information block, which differ in size from trace data information.

Edwards also teaches:

> "and outputting a sequence of the second information blocks from the data processor via a plurality of terminals of the data processor."

as an interfacing step that outputs the trace information stored in the FIFO (storing second information blocks) to an external system though a transmission medium (Edwards: Col. 7 Lines 31-38, Fig.2 Elements: 205, 202, 212, 213, 215, 106) though the plurality of terminals of data processor (Edwards: Fig.2, Element: 205). Details of the transmission medium are not provided and hence can include a medium containing plurality of terminals or wire to transfer trace data.

Regarding Claim 2

Edwards teaches that in one embodiment the trace information (first information blocks) is compressed before being stored in FIFO (representing & storing second information blocks). Thus the size of second information block is smaller than first information blocks (Edwards: Col.9, Lines 55-60).

Regarding Claim 3

Edwards teaches that trace information present in the FIFO might contain other control information like timing, program counter and address data in a compressed format (Edwards: Col.18, Lines 44-49). An embodiment of compression code is also shown (Edwards: Col.19, Lines 20-59). This data is exported the debug tool on the external system (Edwards: Col.6, Lines 33-35) the tool reconstructs the message and control information (Edwards: Col.19, Lines 18-20).

Regarding Claim 4

Edwards teaches that first information block may be packets on a switched communication medium (Edwards: Col.5, Lines 43-46) and second information blocks are made from first information blocks and are inform of packets (Edwards: Col.8, Lines 58-60; Col.7, Lines 31-38) to be sent to an external system over a transmission circuit.

Claim 8-9

Edwards teaches that trace information can be stored in any format and any number of intervals in trace buffer (storing equivalent of first information blocks) (Edwards: Col 17, Lines 48-52) limited to 3*64 bit words. This information is then stored in the

FIFO. Trace data is then extracted with one trace message at a time, which is held trace port registers (one or more) to hold multiple trace buffer packets (1st Information blocks) making one trace message (2nd Information blocks)(Edwards: Col 17, Lines 61-67), before being sent to external system (Edwards: Col.18, Lines 1-5). One or all the packets can be composed of the more than one trace buffer packet.

Regarding Claim 15

Edwards teaches that the debug system (emulation controller) sends reference frames during idle periods to the host system (Edwards: Col.20, Lines 26-33). There is no emulation data except timing information indicating current time in debug system exchanged (Edwards: Col.20, Lines 12-14). This is equivalent to the NOP blocks sent into the sequence of trace message (second information blocks).

Regarding Claim 16

Apparatus of claim 16 performs and is directed at the same functionality as the method of claim 1 and is thus rejected in the like manner. A data processor in the claim 16 is equivalent to data processor in claim 1. A collector in claim 16 is performing the same step of the method as the collection process in the claim 1. An exporter in claim 16 (coupled to the collector) performs the function of receiving trace data (from collector) and re-arranging trace data, as in method-step of claim 1. An exporter coupled to plurality of terminals to output the data is performing the same function as "outputting in sequence" step in claim 1. Further claim 16 states that all these components are part of an integrated circuit. Edwards teaches that

data processor, collector and exporter can be on the same integrated circuit (Edwards: Fig.1, Element 101).

Regarding Claim 17

Apparatus claim 17 is directed at the same functionality as the method claim 2 and is thus rejected in the like manner.

Regarding Claim 27

System of claim 27 performs and is directed at the same functionality as the method of claim 1 and is thus rejected in the like manner. Edwards teaches that data processor (Edwards: Fig.1, Element 102), emulation controller (Edwards: Fig.1, Element 103-Debug unit), apparatus to convey emulation information between processor and emulation controller (Edwards: Fig.2, Element 227 (trace buffer), 220(capture buffer), 206(trace data latch)) and exporter (Edwards: Fig.2, Element 215, 106) can be on the same integrated circuit (Edwards: Fig.1, Element 101). An exporter coupled to plurality of terminals to exporter the data is performing the same function as "outputting information" step in claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claim 5-7, 10-14, 18-26, 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. US Patent No 6,732,307 issued to Edwards in view of "The IBM 8209 LAN Bridge" by Latif et al.

   Regarding Claims 5 & 6

   Teachings of Edwards are disclosed above in claim 1 & 4 rejections. Edwards teaches that information can be presented in a packet format.

   Edwards does not disclose that one of the second information blocks are formed solely from portions of one of the first information blocks.

   Latif et al teach an information packet translation method. In this method an Ethernet packet is formed solely from the Token Ring packet (Latif: Page 37, Figure

15). Here one and all second information packets can be translated from first information packets.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to use teachings of teachings of Latif et al and apply them to teachings of Edwards. The motivations comes from the fact that Edwards teaches a emulation/debug circuit that could be connected to various processors and a some mechanism must be required to create proper routing between host system and one/many emulation processors (Edwards: Col.5, Lines 66-67). Further, Latif details that transparent bridging concept assures that end stations have no route awareness (Latif: Page 29, Transparent Bridging concept, Paragraph 1).

Regarding Claim 7

Edwards teaches that aforementioned trace system can be used to convert the rate of transmission (Edwards: Col.2, Lines 37-40).

Edwards does not teach that the second information blocks are transmitted at a higher data rate than rate of reception of first information blocks.

Latif et al teachings are disclosed in claim 5 & 6 rejections above. Latif et al further teach Token Ring (equivalent to First Information Blocks) packets can be transmitted/received at 4 Mb/s and Ethernet packets (equivalent to Second Information Blocks) can be transmitted at 10Mb/s (Latif: Page 33, LAN Speeds, 1st paragraph, Lines 2-5); a much higher rate than First Information Blocks.

Regarding Claims 10

Teachings of Edwards are disclosed in claims 8-9 rejection above.

Edwards does not disclose that second information block is transmitted at lower block rate than sequence of first information block.

Latif et al teaches that Token Ring (equivalent to first information block) can also be transmitted/received at 16 Mb/s compared to Ethernet packets (equivalent to second information block) transmitted at 10Mb/s (Latif: Page 33, LAN Speeds, 1st paragraph, Lines 2-5).

Regarding Claims 11-12

Teachings of Edwards are disclosed in claims 8-9 rejection above. Edwards also teaches that oldest trace message is sent out first in sequence (Edwards: Col. 17, Lines 66-67; Col.18, Lines 1-17). This process is true for all trace messages that extend the trace buffer boundaries (Edwards: Fig.8).

Regarding Claim 13

Claim 13 is directed towards the same subject matter as claim 10 and it is rejected for the same reasons.

Regarding Claim 14

Edwards teaches that FIFO trace message assembled into trace port registers (Edwards: Fig.2, Element 2 – trace message – 2nd information blocks) can be less than 3*64 bits to read the maximum size of trace entry which may be constructed from multiple trace buffer messages (Edwards: Fig.9, Col.17, Lines 45-52, 61-66).

Hence it can be seen the data size of second information block (trace message in trace port register) is greater than the size of the first information block (trace buffer message).

Regarding Claim 18

Apparatus claim, claim 18 is directed towards the same subject matter as the method claim 5. Hence it is rejected for the same reasons as claim 5.

Regarding Claim 19

Apparatus claim, claim 19 is directed towards the same subject matter as the method claim 7. Hence it is rejected for the same reasons as claim 7.

Regarding Claim 20

Apparatus claim, claim 20 is directed towards the same subject matter as the method claim 8. Hence it is rejected for the same reasons as claim 8.

Regarding Claim 21

Apparatus claim, claim 21 is directed towards the same subject matter as the method claim 10. Hence it is rejected for the same reasons as claim 10.

Regarding Claim 22

Apparatus claim, claim 22 is directed towards the same subject matter as the method claim 14. Hence it is rejected for the same reasons as claim 14.

Regarding Claim 23

Apparatus claim, claim 23 is directed towards the same subject matter as the method claim 11. Hence it is rejected for the same reasons as claim 11.

Regarding Claim 24

Apparatus claim, claim 24 is directed towards the same subject matter as the method claim 13. Hence it is rejected for the same reasons as claim 13.

Regarding Claim 25

Teachings of Edwards are disclosed above in claims 23, 20 & 16. Edwards also discloses that exporter (part of debug apparatus - Edwards: Fig.2, Element 103) stores the first information blocks in Capture Buffer (Edwards: Fig.2, Element 203) and Trace Data Latch (Edwards: Fig.2, Element 206).

Regarding Claim 26

Apparatus claim, claim 26 is directed towards the same subject matter as the method claim 14. Hence it is rejected for the same reasons as claim 14.

Regarding Claims 28 & 29

Teachings of Edwards are disclosed above in claims 27. Edwards also teaches that the debug system (emulation controller) is connected to external system (Edwards: Col.6, Lines 12-14). An external system could be a host computer running the debug tool mentioned by Edwards (Edwards: Col 7, Lines 46-48). A keyboard constitutes a "tactile interface" and a computer monitor constitutes a "visual interface". Official notice is taken that it is extremely well known in the art to use a keyboard and a computer monitor with a computer (host interface) to form a man-machine interface.

Remarks

All claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

as

JEAN R. HOMERE
PRIMARY EXAMINER